CLAIMS

WE CLAIM:

1. A semiconducting device adapted to prevent and/or to thwart reverse engineering, including:

(a) an insulating layer disposed on a semiconductor substrate;

(b) a first metal layer and a second metal layer, said first metal layer and second metal layer being separated by said insulating layer; and

(c) a via defined by said insulating layer, said via having a first end and a second end,

wherein said first end of said via is connected to said first metal layer and said second end of said via terminates prior to reaching said second metal layer.

2. The device as claimed in Claim 1, wherein said semiconducting device comprises an integrated circuit.

3. The device as claimed in Claim 1, wherein said insulating layer further comprises silicon oxide.

4. The device as claimed in Claim 2, wherein said integrated circuit further comprises complementary metal oxide-semiconductor, bipolar silicon, or group III-group V integrated circuits.

5. A semiconducting device adapted to prevent and/or to thwart reverse engineering, including:

(a) an insulating layer disposed on top of semiconductor substrate;

(b) a first metal layer and a second metal layer, said first metal layer and second metal layer being separated by said insulating layer; and

(c) a via defined by said insulating layer, said via having a first end and a second end,

wherein said second end of said via is connected to said second metal layer and said first end of said via terminates prior to reaching said first metal layer.

6. The device as claimed in Claim 5, wherein said semiconducting device comprises an integrated circuit.

7. The device as claimed in Claim 5, wherein said insulating layer further comprises silicon oxide.

8. The device as claimed in Claim 6, wherein said integrated circuits further comprise complementary metal oxide-semiconductor, bi-polar silicon, or group III-group V integrated circuits.

9. A method for preventing and/or thwarting reverse engineering, comprising steps of:

(a) disposing an insulating layer on top of semiconductor substrate;

(b) forming and patterning a first metal layer and a second metal layer so that said first metal layer and said second metal layer are separated by said insulating layer; and

(c) forming a via defined by said insulating layer, said via having a first end and a second end,

wherein said first end of said via is connected to said first metal layer and said second end of said via terminates prior to reaching said second metal layer.

10. The method as claimed in Claim 9, wherein said semiconducting device comprises integrated circuits.

11. The method as claimed in Claim 9, wherein said insulating layer further comprises silicon oxide.

12. The method as claimed in Claim 10, wherein said integrated

circuits further comprise complementary metal oxide-semiconductor, bi-polar silicon, or group III-group V integrated circuits.

13. A method for preventing and/or thwarting reverse engineering, comprising steps of:

(a) disposing an insulating layer on top of semiconductor substrate;

(b) forming and patterning a first metal layer and a second metal layer so that said first metal layer and said second metal layer are separated by said insulating layer; and

(c) forming a via defined by said insulating layer, said via having a first end and a second end,

wherein said second end of said via is connected to said second metal layer and said first end of said via terminates prior to reaching said first metal layer.

14. The device as claimed in Claim 13, wherein said semiconducting device comprises integrated circuits.

15. The device as claimed in Claim 13, wherein said insulating layer further comprises silicon oxide.

16. The device as claimed in Claim 14, wherein said integrated circuits further comprise complementary metal oxide-semiconductor,

bi-polar silicon, or group III-group V integrated circuits.